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ABSTRACT

A signal processor that contains a programmable logic circuitry that is re-configurable in response to various parameters including, but not limited to, characteristics of a plurality of input data that is provided to the signal processor. The signal processor contains, among other things, a programmable logic configuration circuitry that provides a logic configuration to the programmable logic circuitry. In certain embodiments of the invention, the signal processor employs a wide word width to program the programmable logic circuitry, the wide word width is operable to configure an entirety of the programmable logic circuitry. The programmable logic configuration circuitry further contains a default configuration circuitry and an adaptive configuration circuitry. The default configuration circuitry contains a default logic configuration for the programmable logic circuitry. In other embodiments of the invention, the adaptive configuration circuitry generates an adaptive logic configuration for the programmable logic circuitry. The programmable logic circuitry is partitioned into a plurality of areas, each area within the plurality of areas is independently programmable.